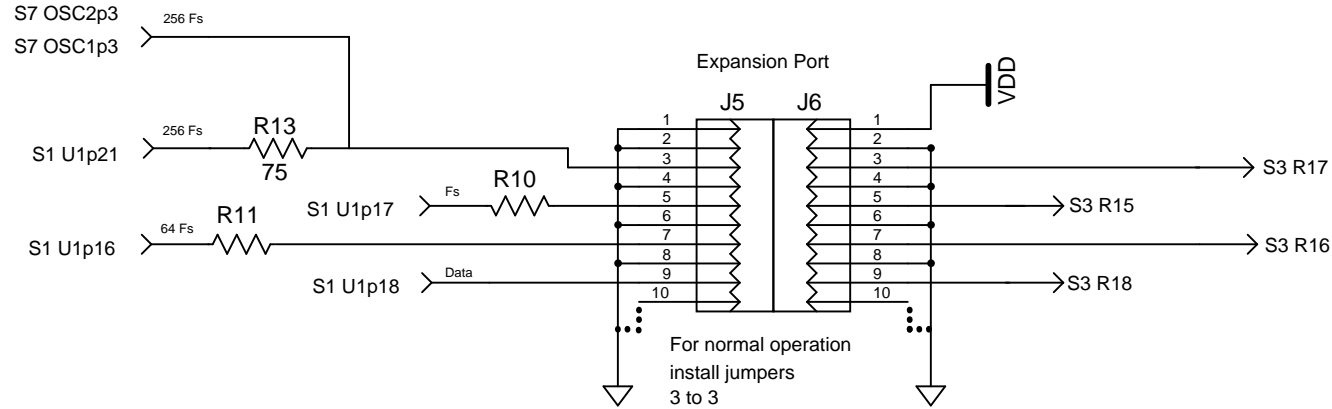
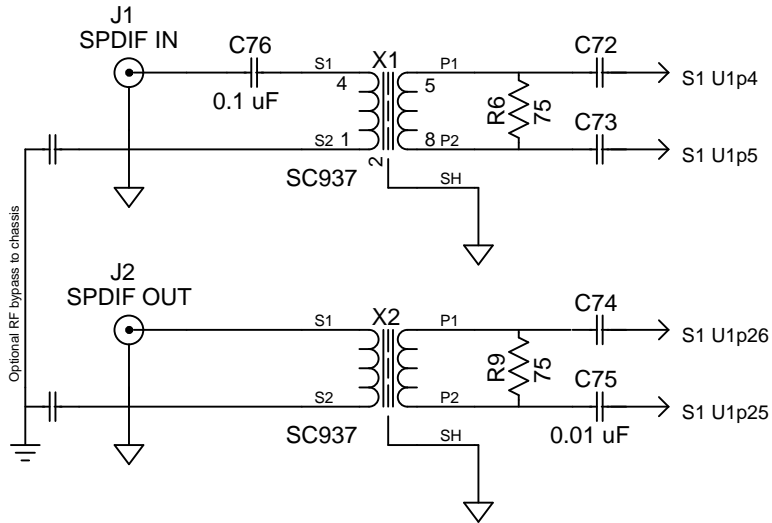
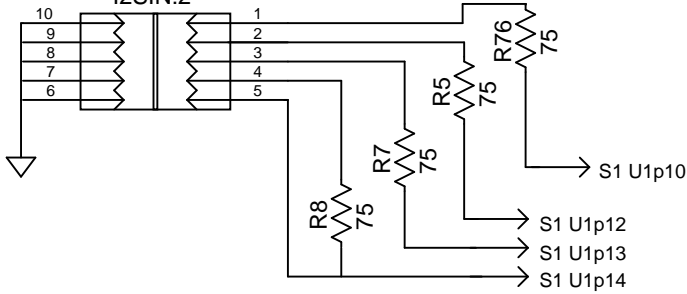
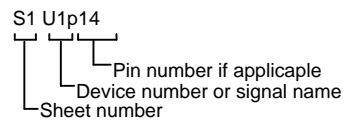




1 = Clock Out in Syncro Mode  
 2-4 I2S Inputs  
 5-6 Mode Jumper  
 I2SIN:2



Sheet In/Out label scheme



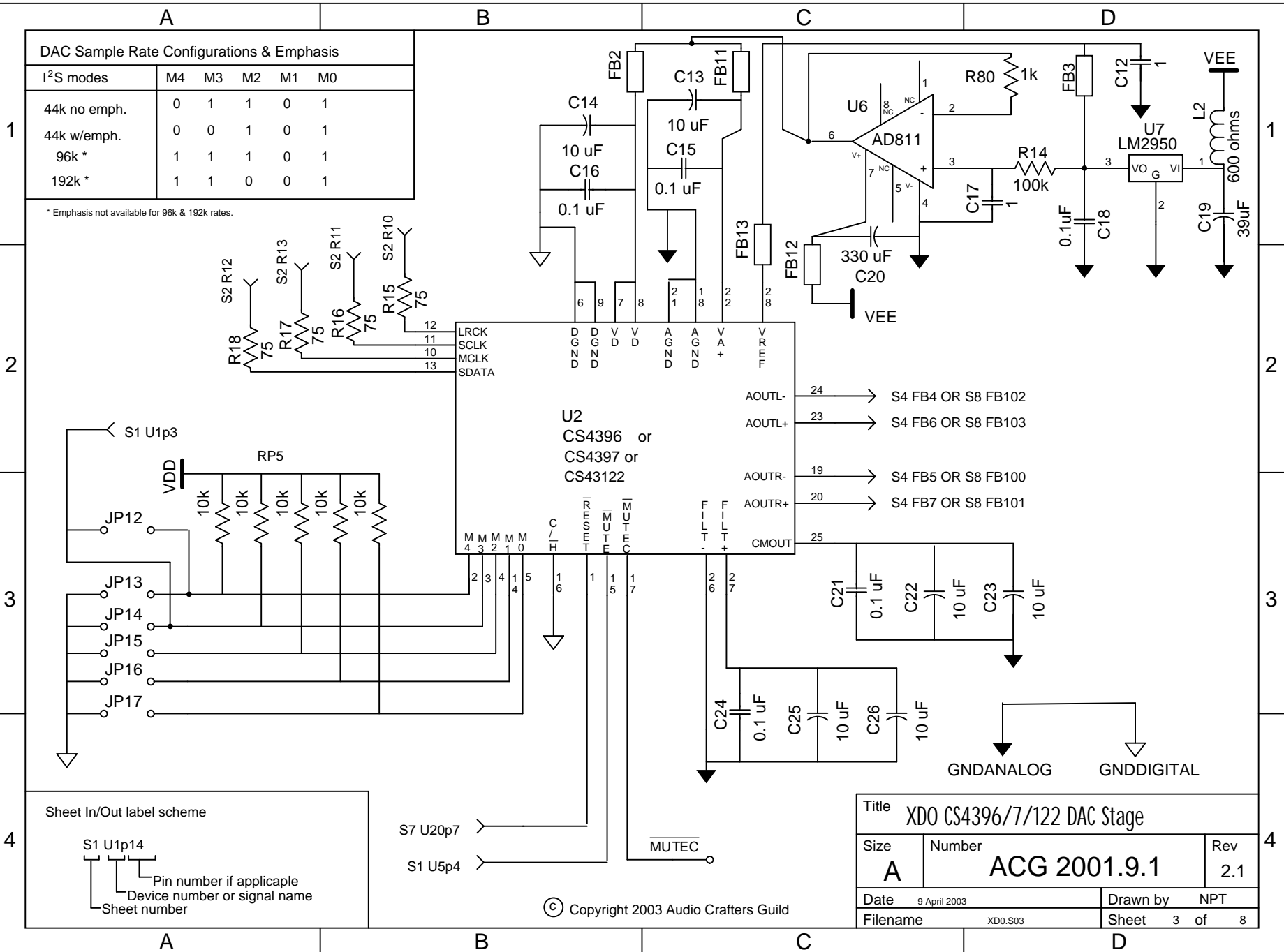
For normal operation  
 install jumpers  
 3 to 3  
 5 to 5  
 7 to 7  
 9 to 9  
 Ground jumpers to pins 10 may  
 be cut if spare I/O pins are needed.

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Title XDO Digital I/O Connections		
Size A	Number ACG 2001.9.1	Rev 2.1
Date 9 April 2003	Drawn by NPT	
Filename XDO.S02	Sheet 2 of 8	

DAC Sample Rate Configurations & Emphasis					
I <sup>2</sup> S modes	M4	M3	M2	M1	M0
44k no emph.	0	1	1	0	1
44k w/emph.	0	0	1	0	1
96k *	1	1	1	0	1
192k *	1	1	0	0	1

\* Emphasis not available for 96k & 192k rates.



1

2

3

4

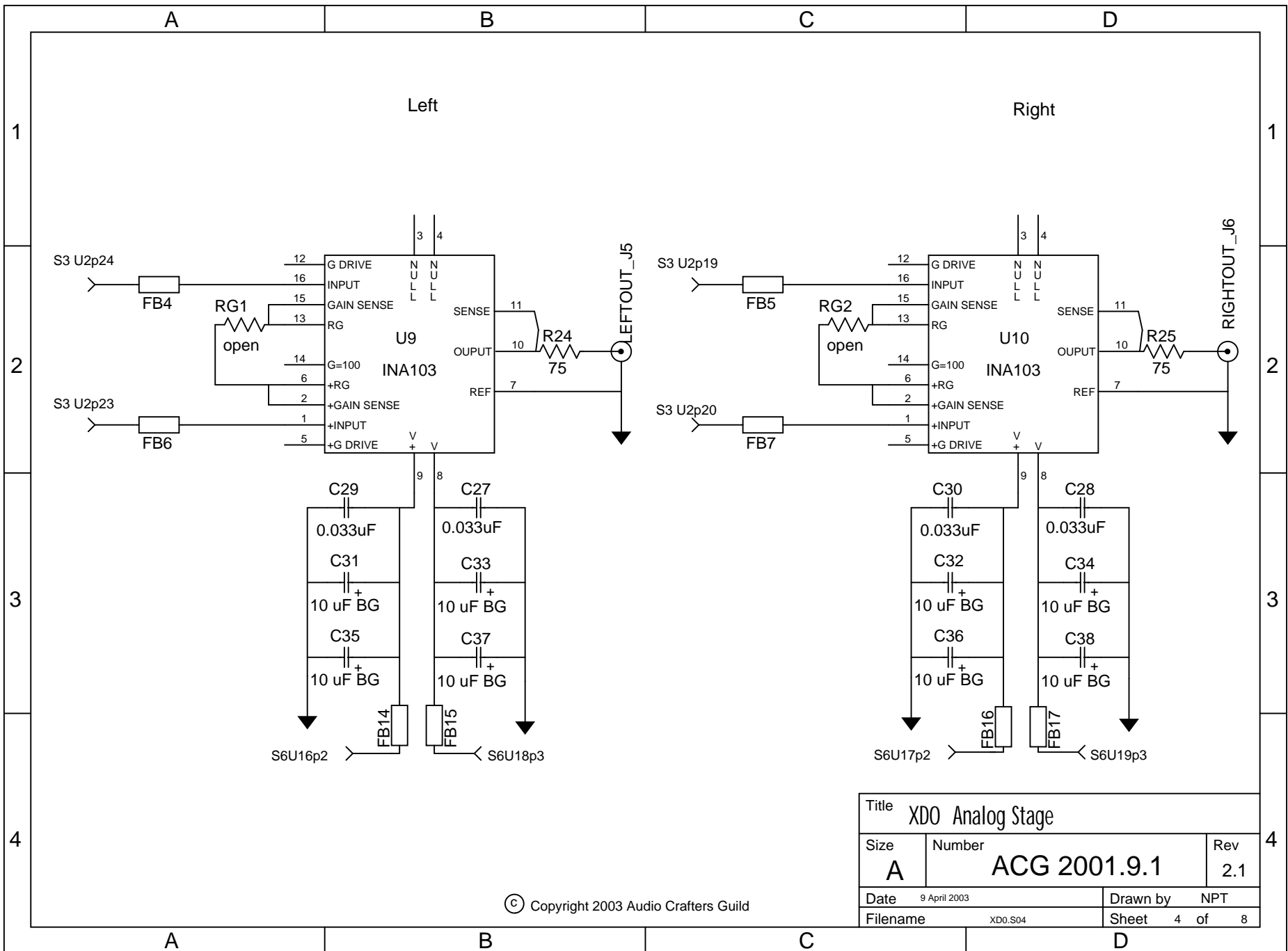
1

2

3

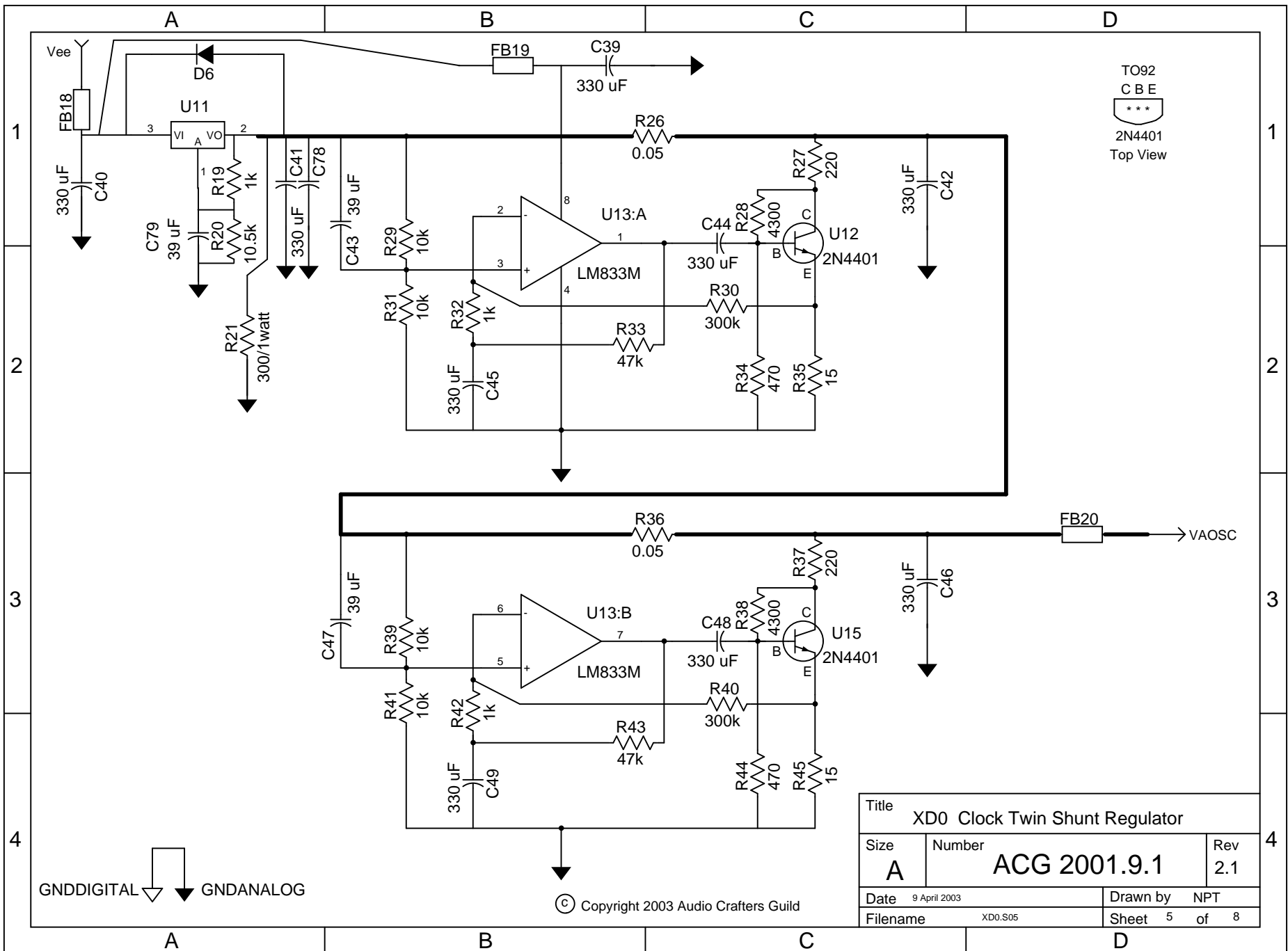
4

Title XDO CS4396/7/122 DAC Stage		
Size A	Number ACG 2001.9.1	Rev 2.1
Date 9 April 2003	Drawn by NPT	
Filename XD0.S03	Sheet 3 of 8	



Title XDO Analog Stage		
Size A	Number ACG 2001.9.1	Rev 2.1
Date 9 April 2003	Drawn by NPT	
Filename XD0.S04	Sheet 4 of 8	

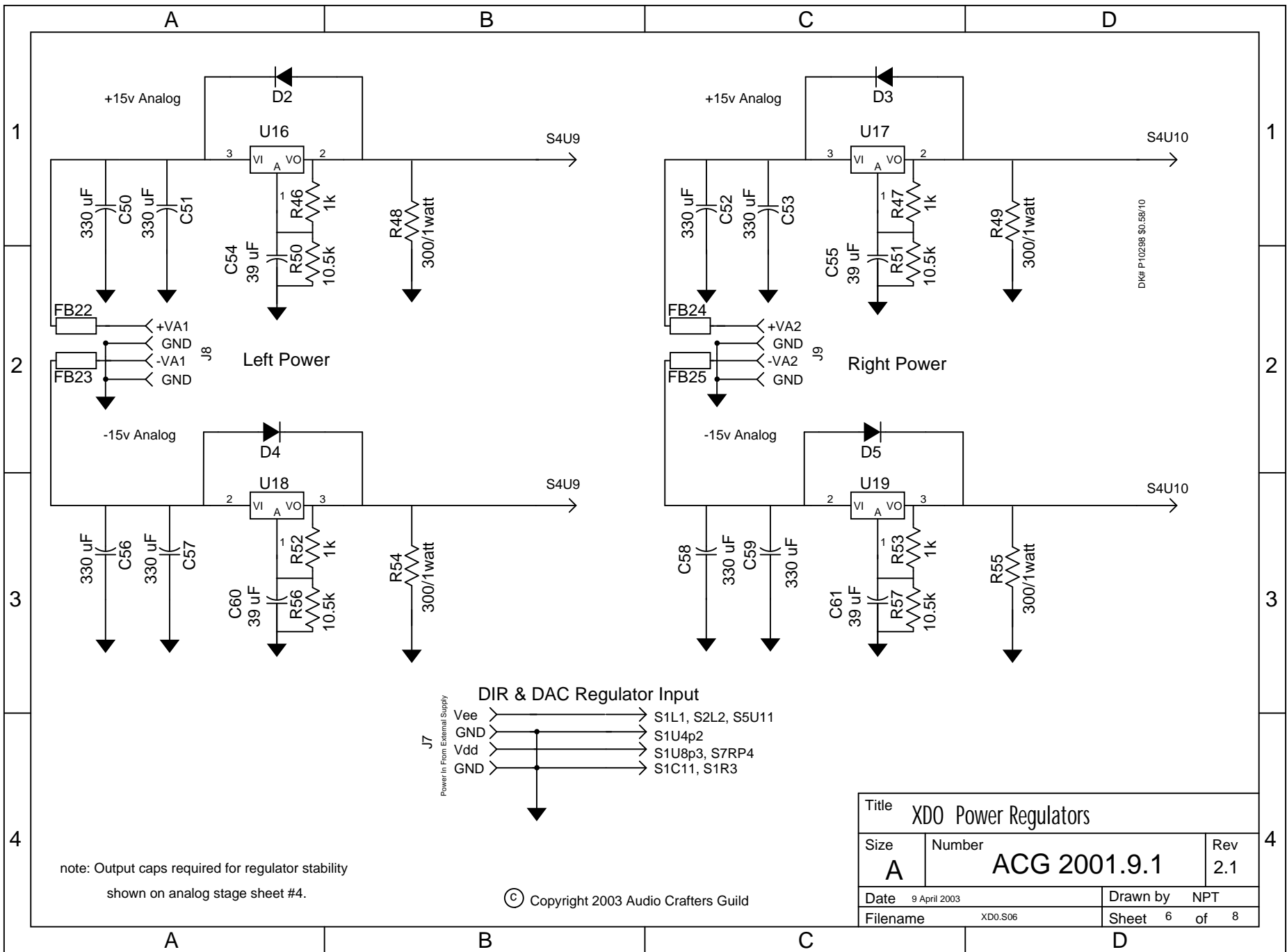
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TO92  
C B E  
\*\*\*  
2N4401  
Top View

Title			XD0 Clock Twin Shunt Regulator		
Size	Number		Rev		
A	ACG 2001.9.1		2.1		
Date	9 April 2003		Drawn by	NPT	
Filename	XD0.S05		Sheet	5 of 8	

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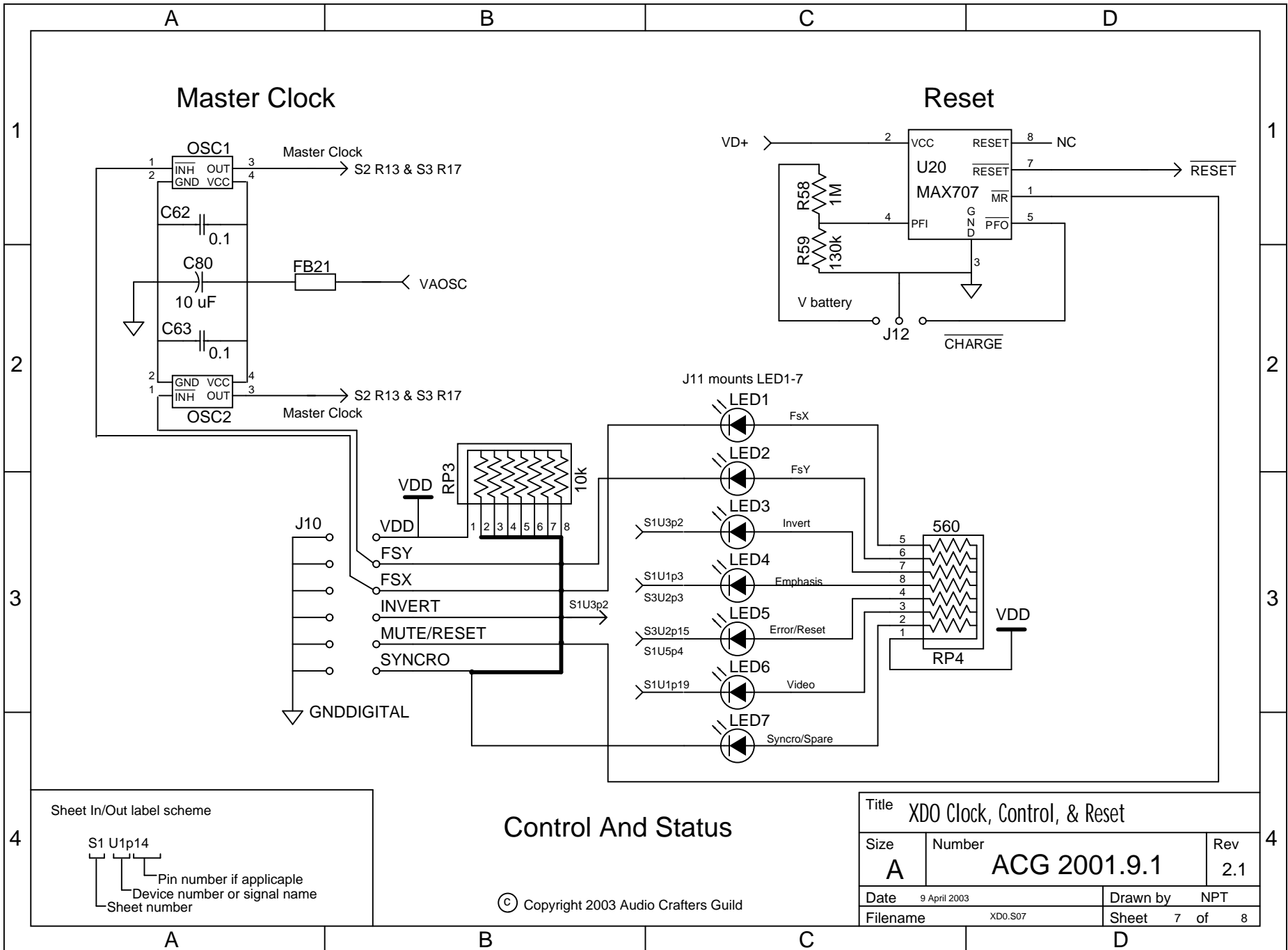


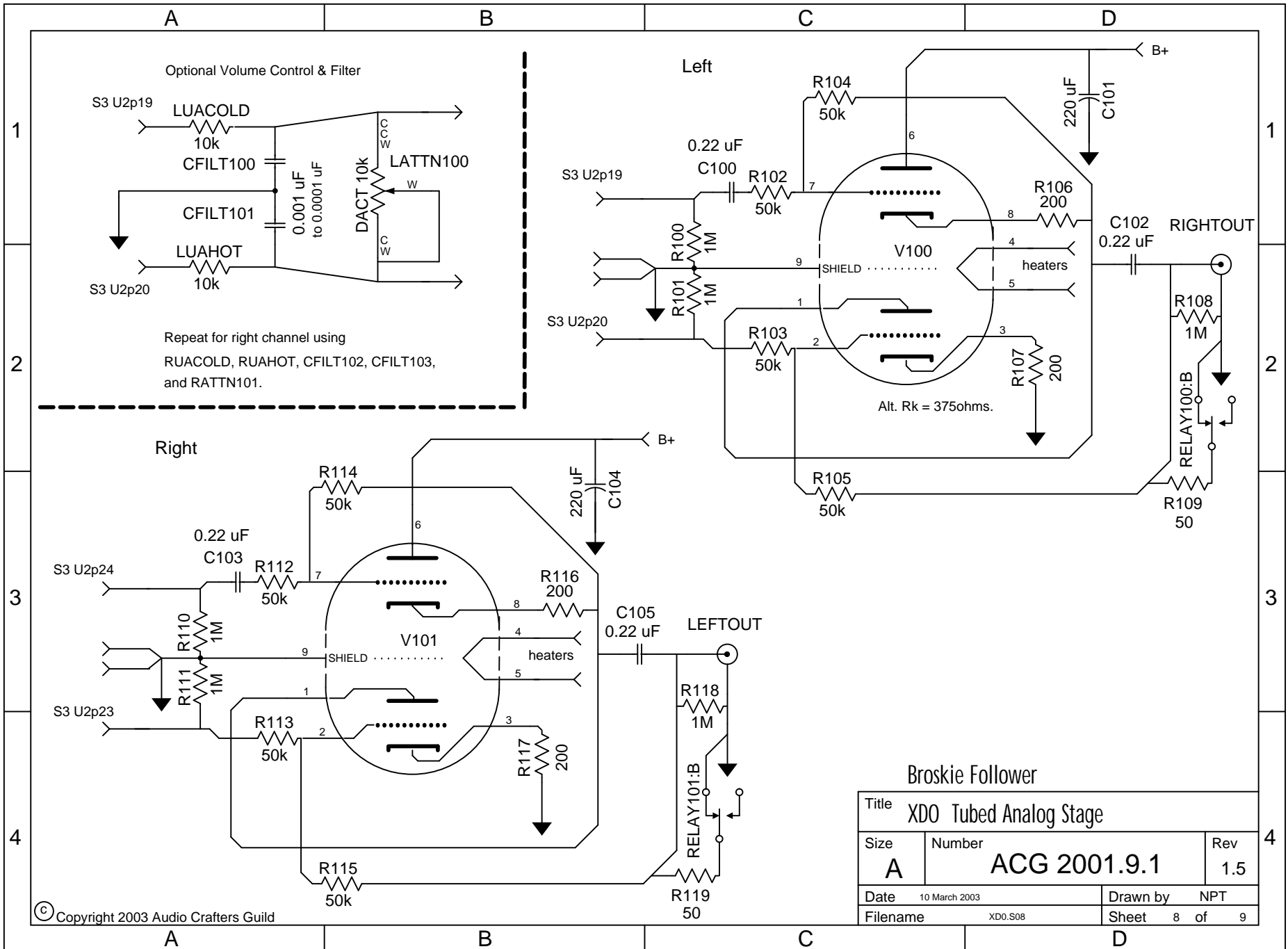
DK# P10298 \$0.58/10

note: Output caps required for regulator stability shown on analog stage sheet #4.

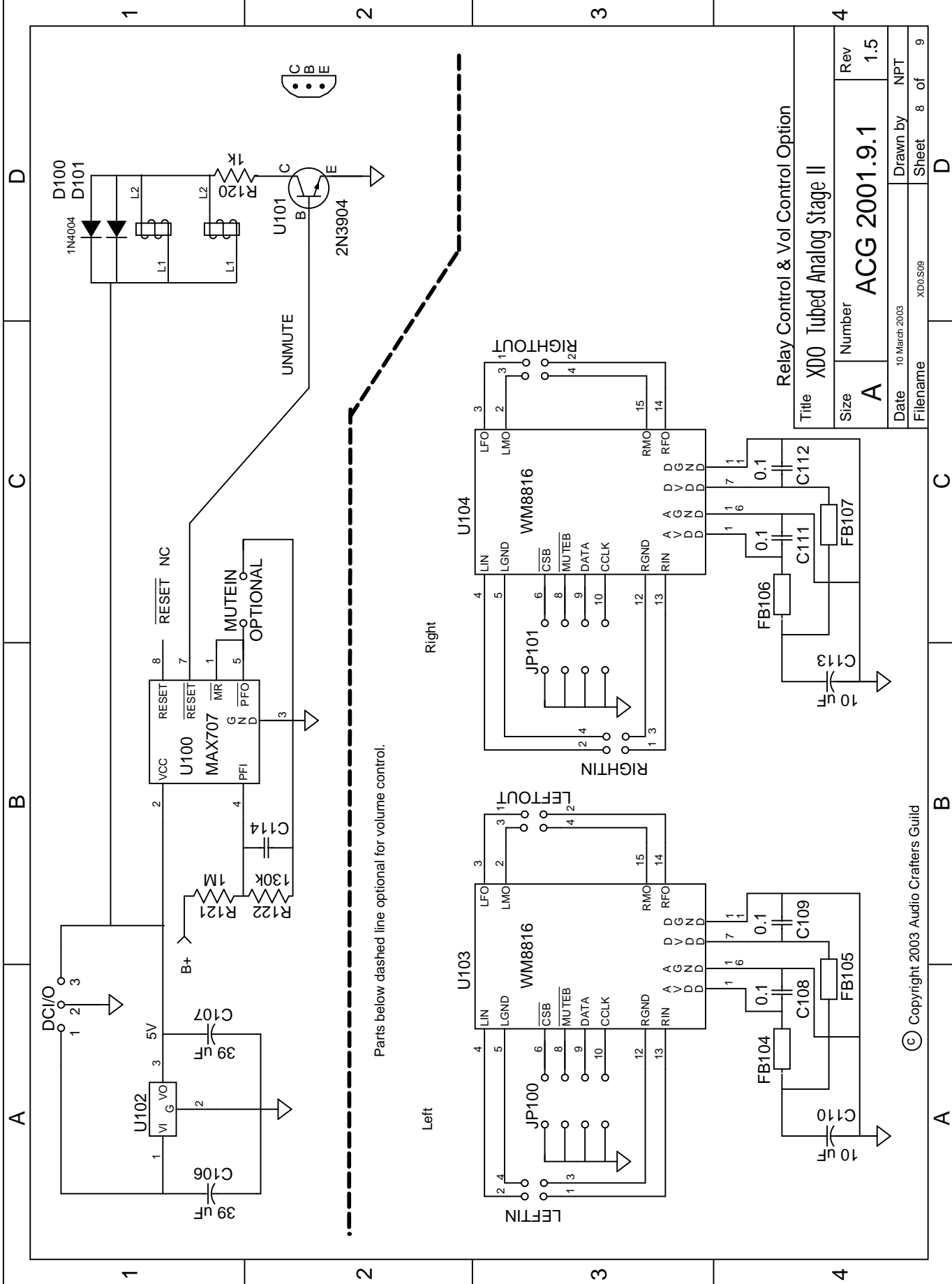
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Title XDO Power Regulators		
Size A	Number ACG 2001.9.1	Rev 2.1
Date 9 April 2003	Drawn by NPT	
Filename XD0.S06	Sheet 6	of 8



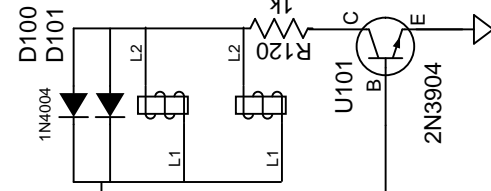






A B C D

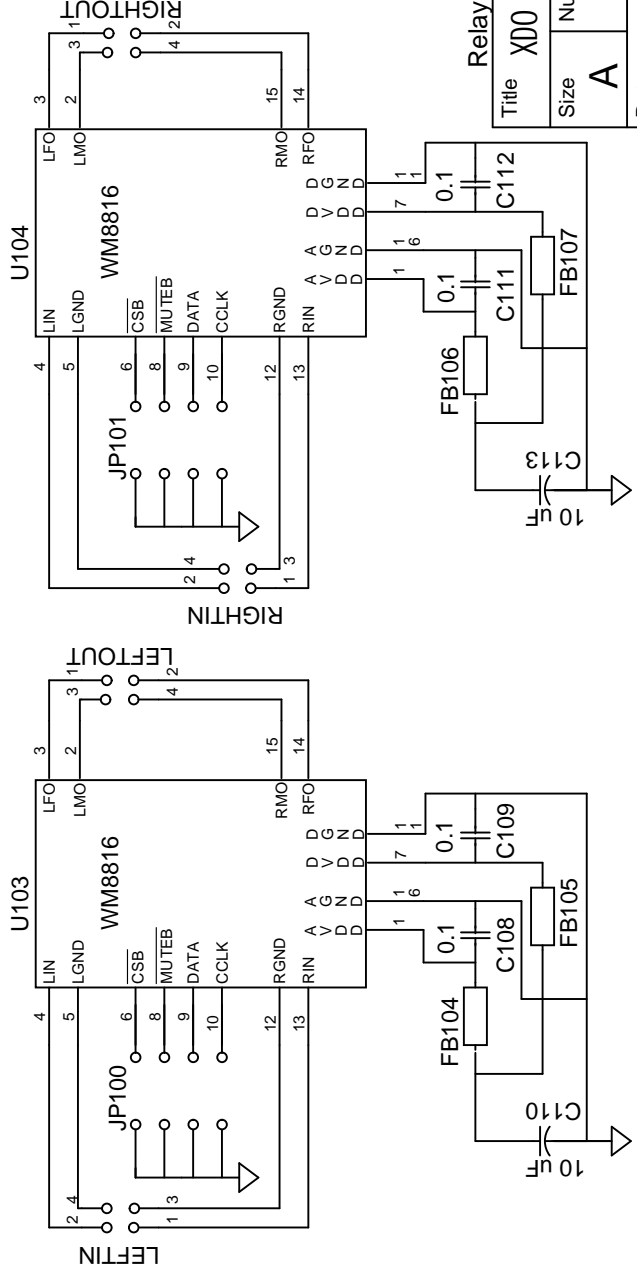
1 2 3 4



Parts below dashed line optional for volume control.

Left

Right



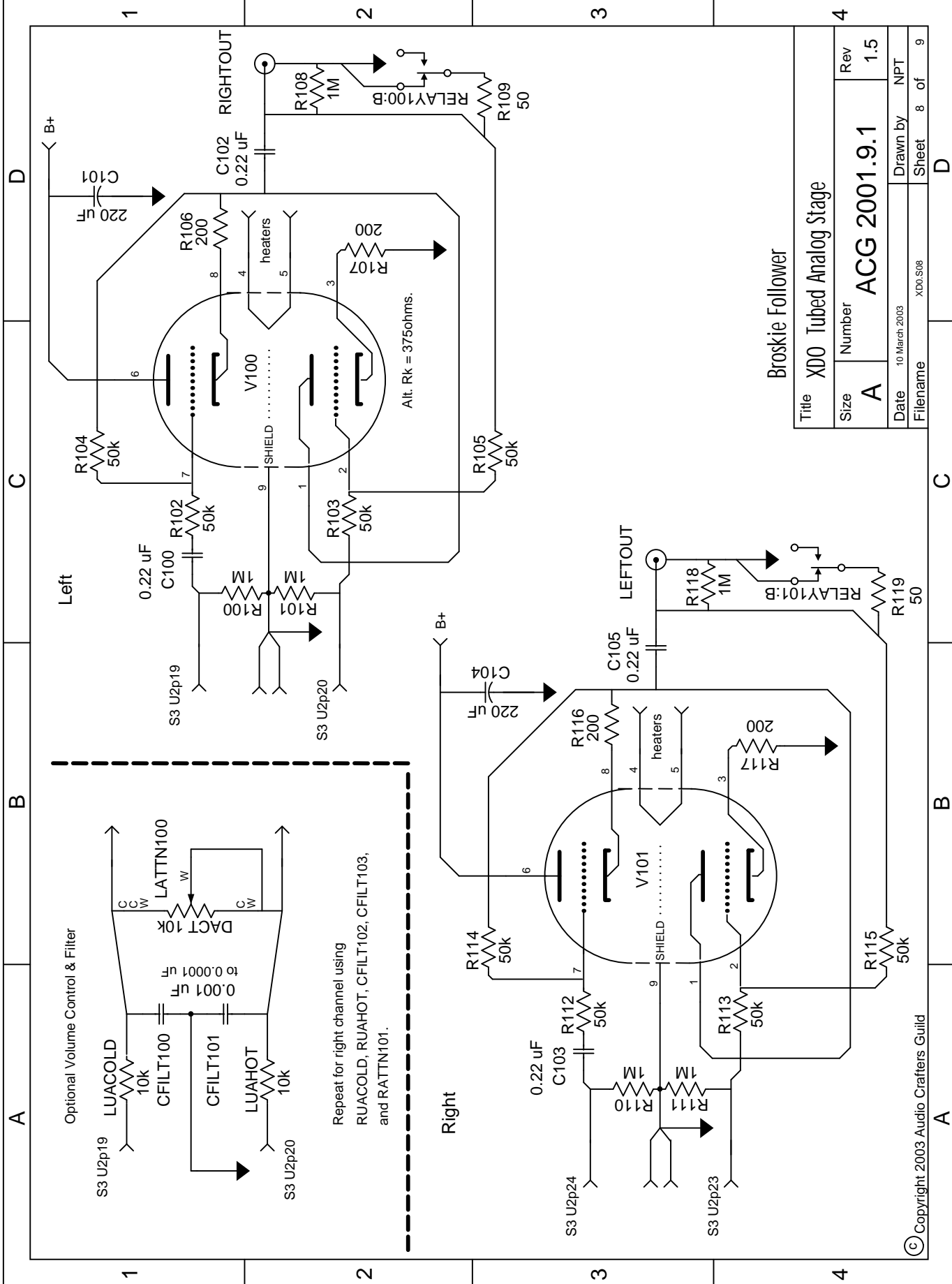
Relay Control & Vol Control Option  
Title XDO Tubed Analog Stage II

Size	A	Rev	1.5
Number	ACG 2001.9.1	Drawn by	NPT
Date	10 March 2003	Sheet	8 of 9
Filename	XD0.S09		

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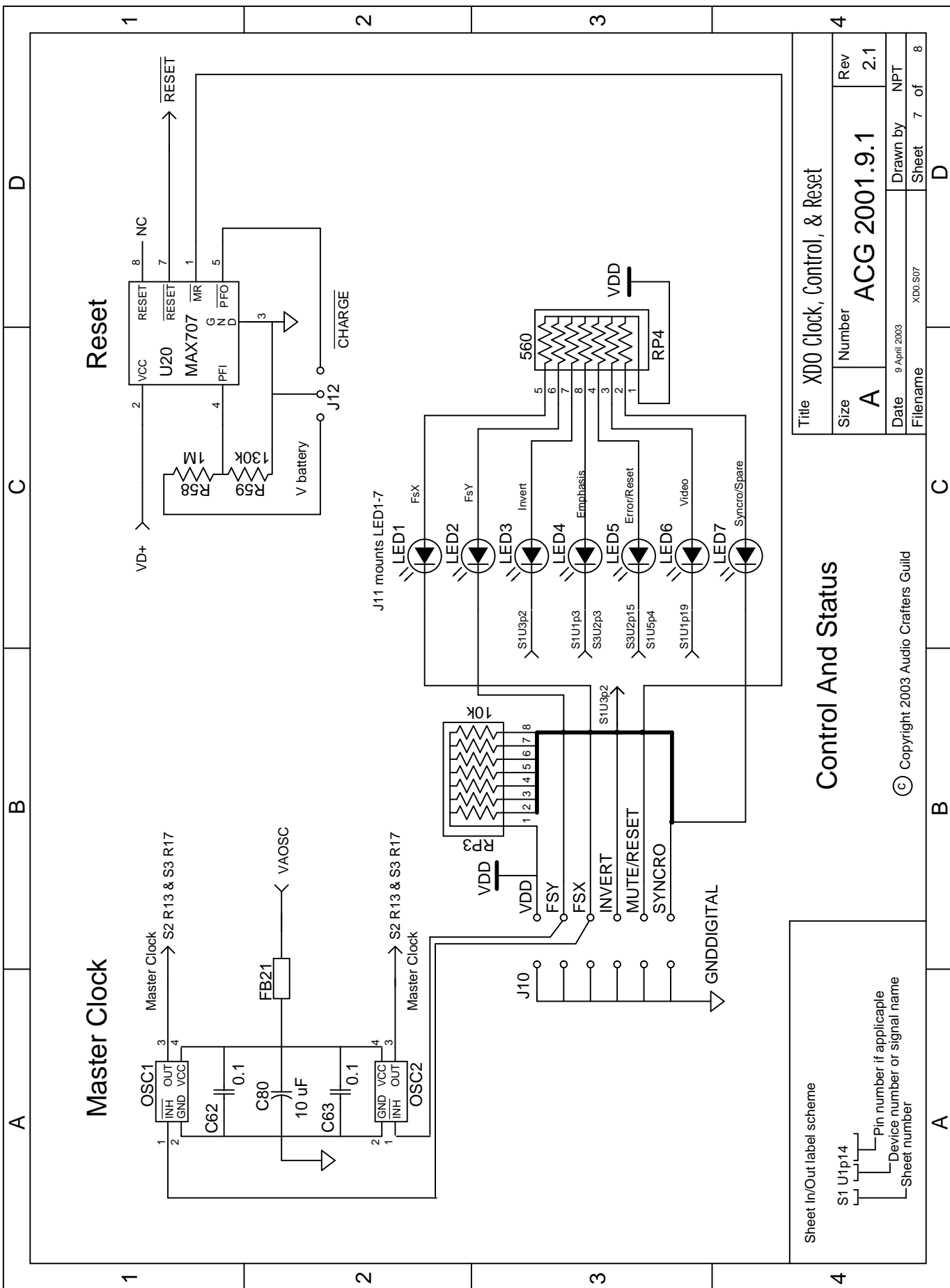
A B C D

1 2 3 4



Broskie Follower

Title		XDO TUBED Analog Stage	
Size	Number	Rev	1.5
A	ACG 2001.9.1	Drawn by	NPT
Date	10 March 2003	Sheet	8 of 9
Filename	XDO.S08		



### Master Clock

### Reset

Sheet In/Out label scheme

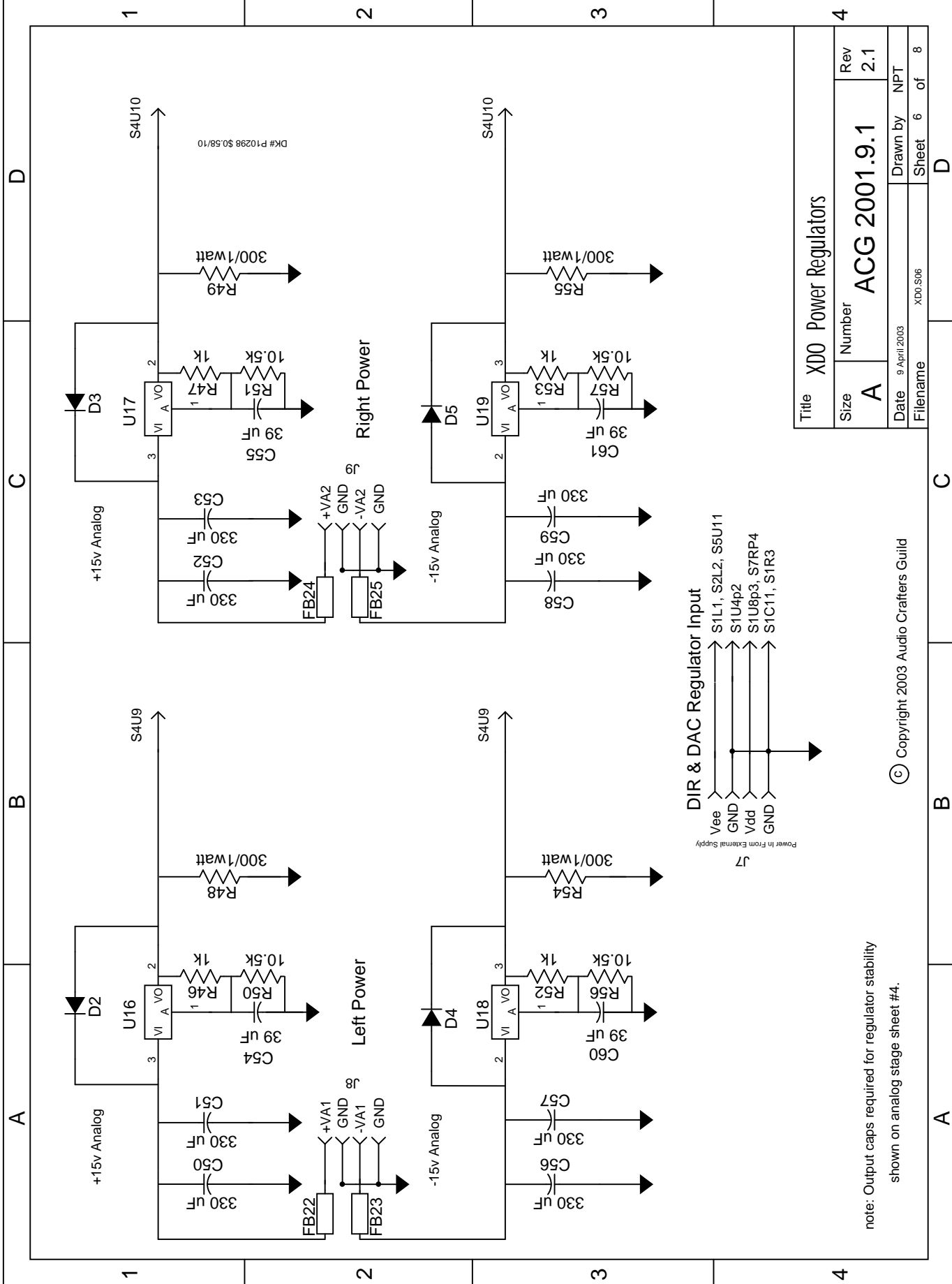
- S1 U1p14
- Pin number if applicable
- Device number or signal name
- Sheet number

### Control And Status

Title XDO Clock, Control, & Reset

Size	Number	Rev
A	ACG 2001.9.1	2.1
Date	Drawn by NPT	
Filename	Sheet 7 of 8	
Date		9 April 2003
Filename		XDO.S07

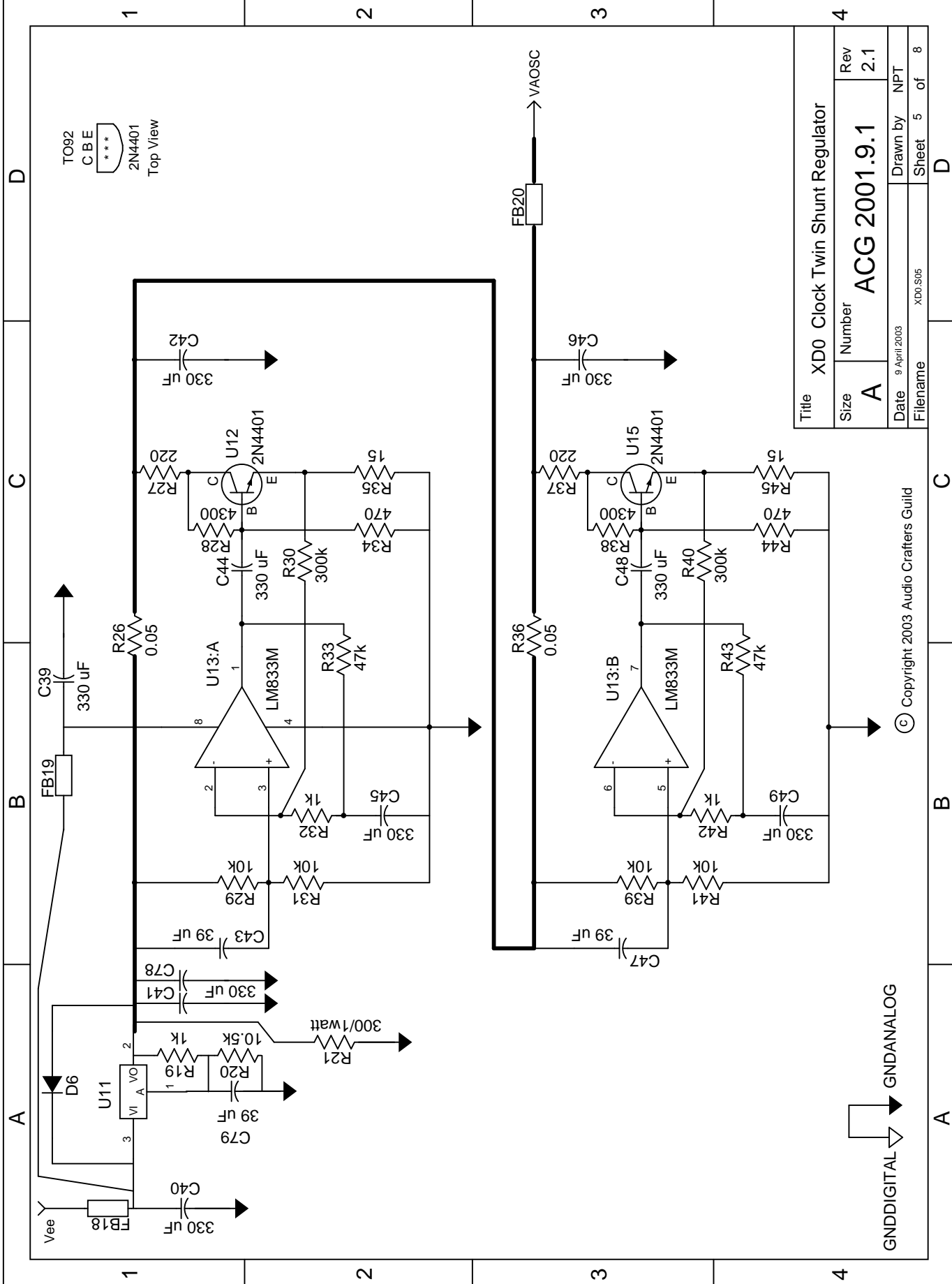
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note: Output caps required for regulator stability shown on analog stage sheet #4.

Title		XDO Power Regulators	
Size	Number	ACG 2001.9.1	Rev
A			2.1
Date	9 April 2003		Drawn by
Filename	XDO.S06		NPT
	Sheet	6	of 8

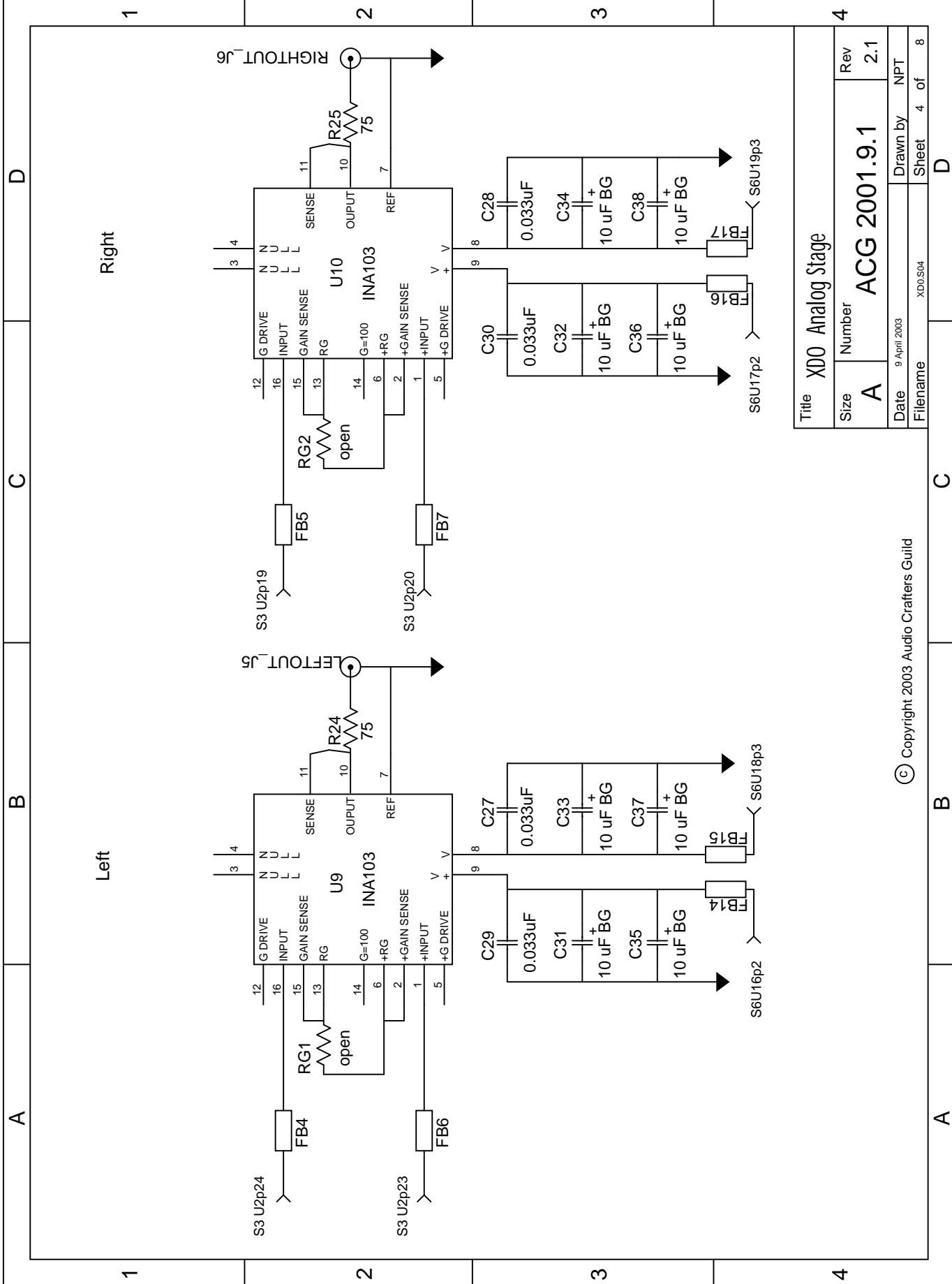
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Title		XDO Clock Twin Shunt Regulator	
Size	Number	Rev	2.1
A	ACG 2001.9.1		
Date	9 April 2003	Drawn by	NPT
Filename	XDO.S05	Sheet	5 of 8

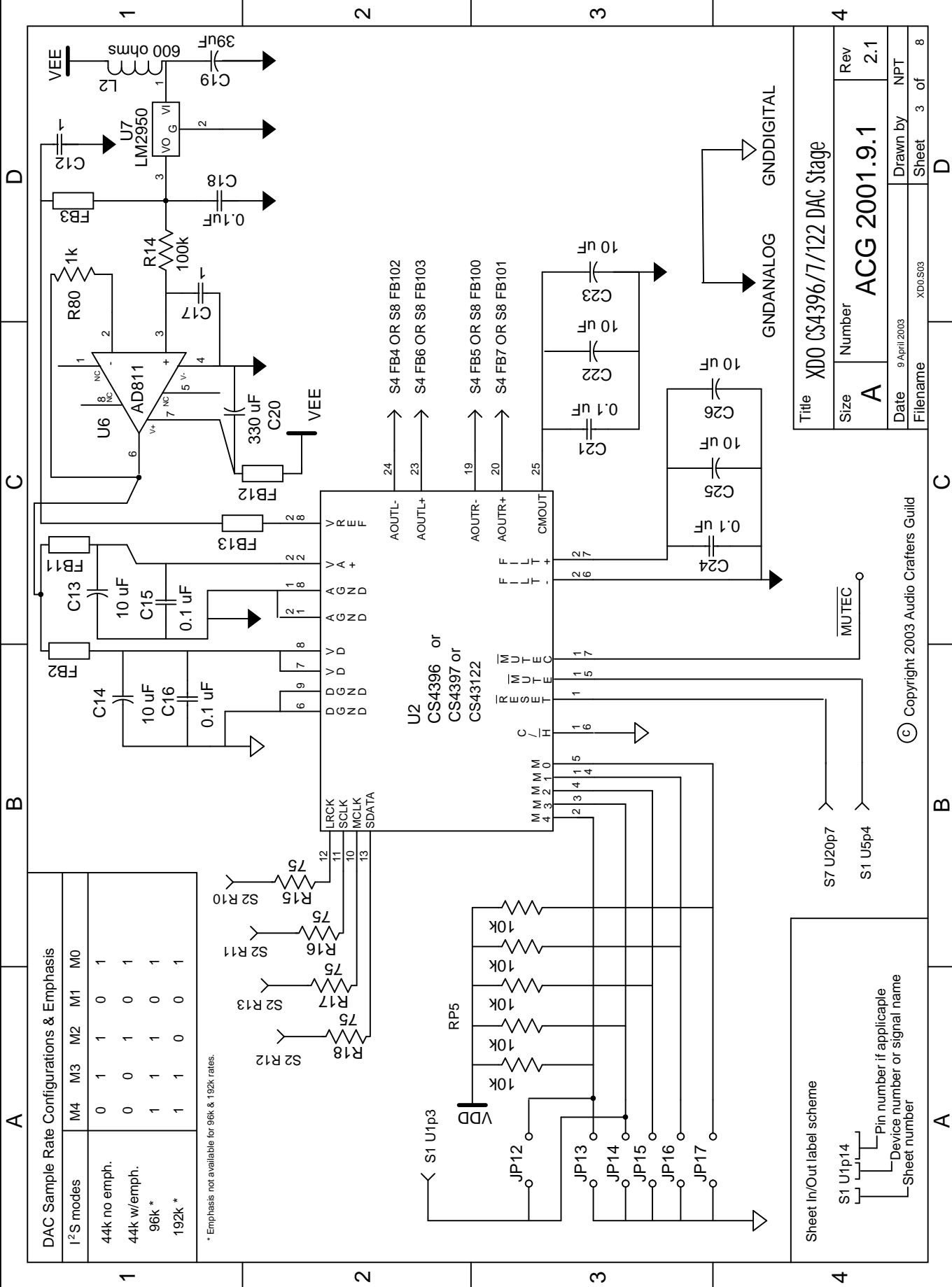
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GNDDIGITAL → GNDANALOG



Title		XDO Analog Stage	
Size	Number	Rev	
A	ACG 2001.9.1	2.1	
Date	9 April 2003	Drawn by	NPT
Filename	XD0.S04	Sheet	4 of 8

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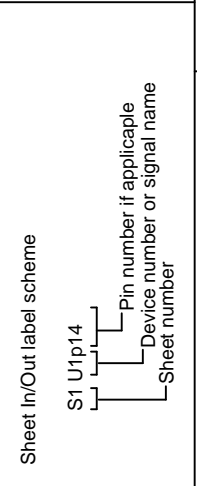
**DAC Sample Rate Configurations & Emphasis**

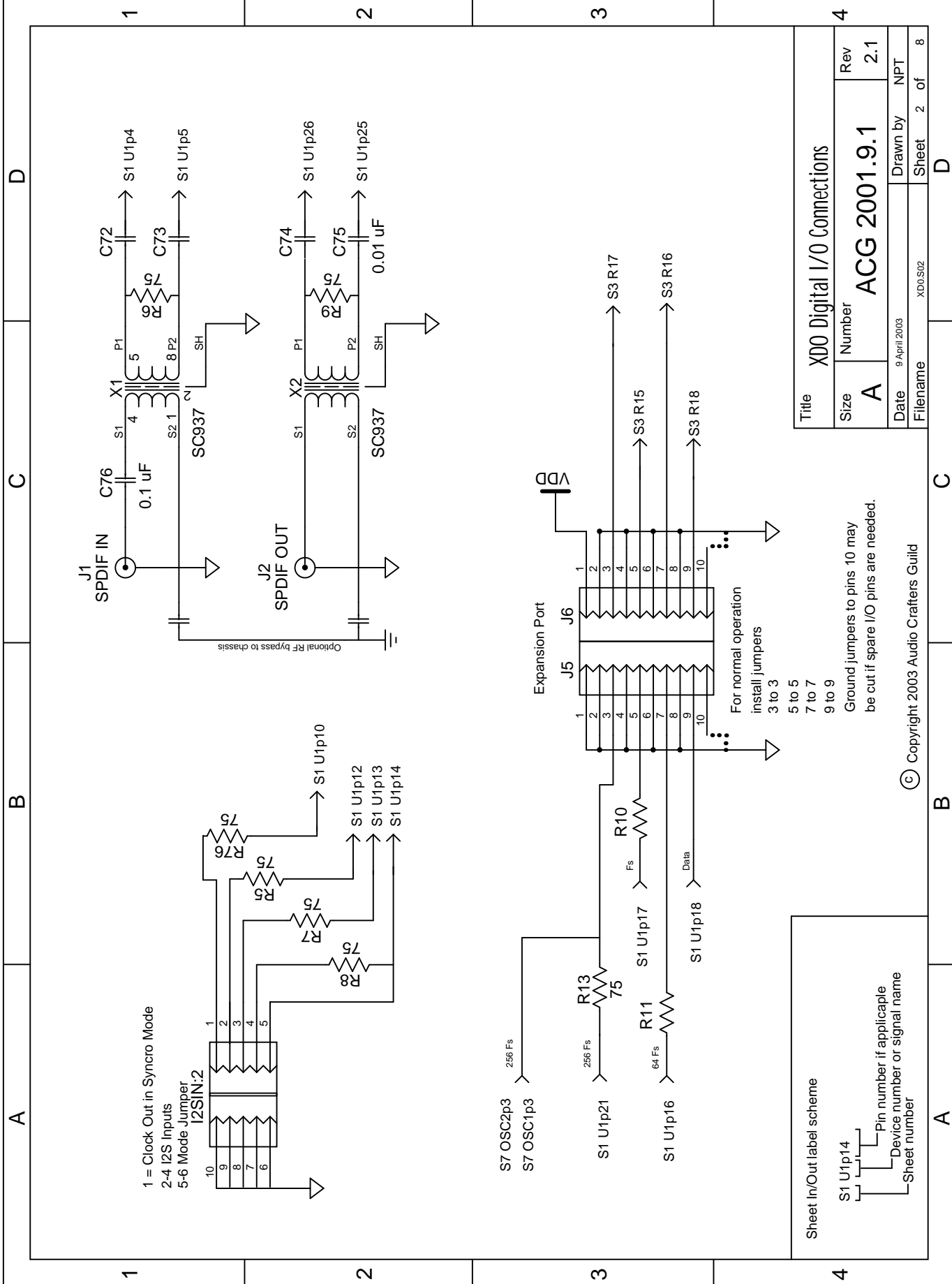
I <sup>2</sup> S modes	M4	M3	M2	M1	M0
44k no emph.	0	1	1	0	1
44k w/emph.	0	0	1	0	1
96k *	1	1	1	0	1
192k *	1	1	0	0	1

\* Emphasis not available for 96k & 192k rates.

Title		XDO CS4396/7/122 DAC Stage	
Size	Number	Rev	2.1
Date	9 April 2003	Drawn by	NPT
Filename	XDO.S03	Sheet	3 of 8

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- 1 = Clock Out in Syncro Mode
- 2-4 I2S Inputs
- 5-6 Mode Jumper
- I2SIN:2

Sheet In/Out label scheme

S1 U1p14

- └─ Pin number if applicable
- └─ Device number or signal name
- └─ Sheet number

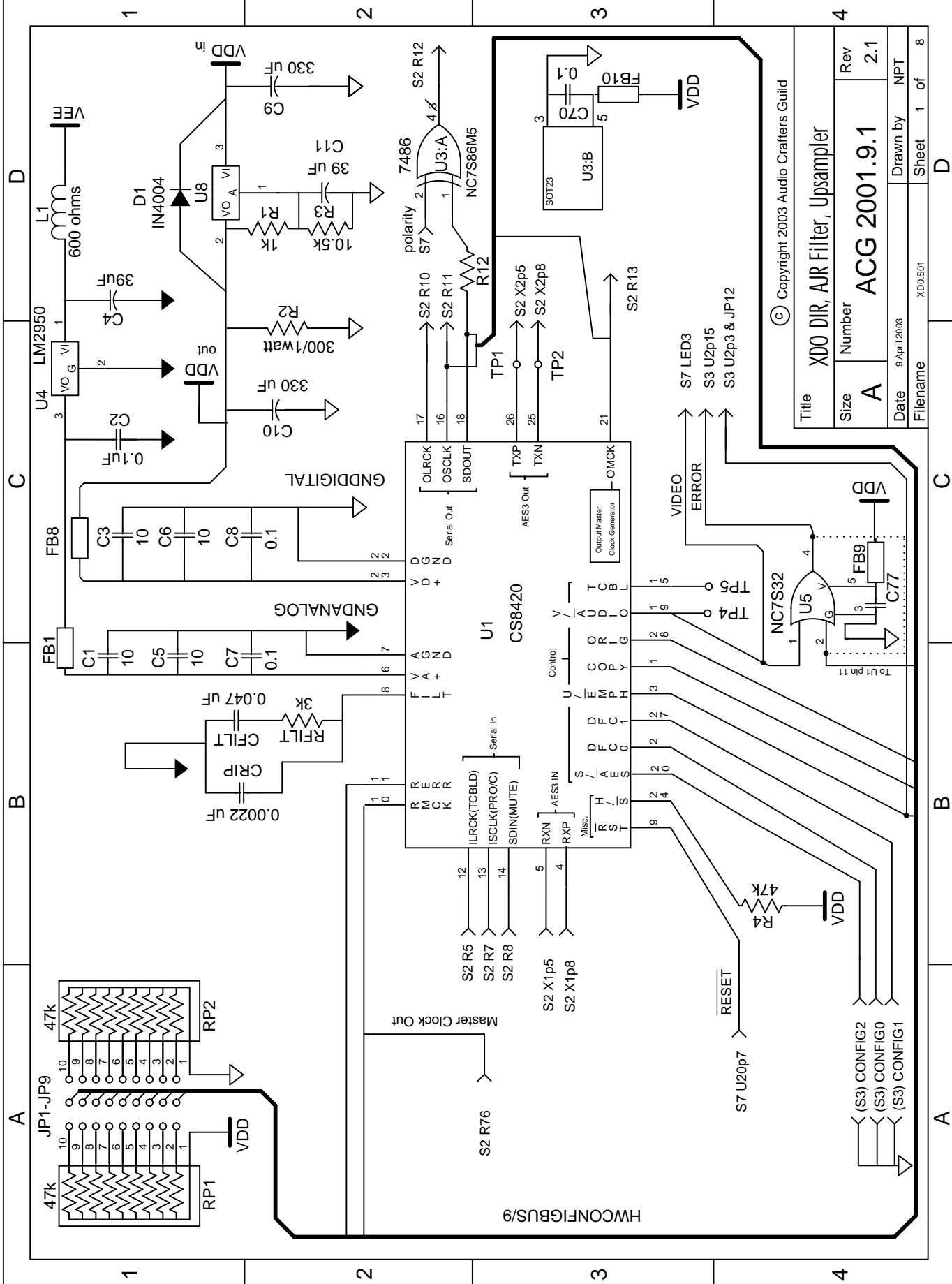
Title		XDO Digital I/O Connections	
Size	Number	Rev	
A	ACG 2001.9.1	2.1	
Date	9 April 2003	Drawn by	NPT
Filename	XD0.S02	Sheet	2 of 8

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Ground jumpers to pins 10 may be cut if spare I/O pins are needed.

For normal operation install jumpers 3 to 3, 5 to 5, 7 to 7, 9 to 9





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Title		XDO DIR, AJR Filter, Upsampler	
Size	Number	Rev	2.1
A		ACG 2001.9.1	
Date	9 April 2003	Drawn by	NPT
Filename	XD0.S01	Sheet	1 of 8

A B C D

