ARCAM

DELTA BLACK BOX 5/50
D/A CONVERTOR
SERVICE MANUAL

BLACK BOX 5/50 SERVICE MANUAL

Issue 1

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CONTENTS

CIRCUIT DESCRIPTION

The Black Box 5 & 50 share common pcbs with virtually identical circuits. The mother board is identical and the digital board has a different DAC (PCM67 on BB5, PCM69 on BB50) and some different values or types of capacitors in various places. The boards can be interchanged without problems. The chassis's on the two units are obviously different and not interchangeable.
The differences on the digital boards between BB5 and BB50 are:

Z207 changed to PCM69 DAC from PCM67
C1,101,220 changed to 10uF non polarised
C216,237 changed to different types of 100uF capacitors
C3,103,4,104 removed.

DIGITAL BOARD

The circuit function is to receive SPDIF format digital audio signals with a sampling rate of 32, 44.1 or 48KHz and decode them into high fidelity analogue audio signals. Provision is provided to synchronize an external SPDIF source to an XTAL clock local to this decoder board via an optical clock output.

SPDIF Receiver

The digital audio signal is received by either Z201 via the coaxial input or Z202 via the optical input. Z203 selects which one is being used and drives the selected signal back to the digital output, SK2 via L201. The selected signal is then processed by Z205, the YM3623B Digital Audio Interface Receiver.

Z205 decodes the data from SPDIF format into serial data. It also extracts synchronizing clock signals from the data using a phase lock loop. When no data is present, the phase locked loop is switched off and an XTAL oscillator, X201, takes over, this is *not* the XTAL oscillator referred to as 'internal XTAL clock'. This keeps the decoder running without producing any glitches which may become audible via the DAC.

Z205 also extracts some status bits from the SPDIF data, these are pre-emphasis and bits indicating the sampling rate, 32, 44.1 or 48KHz. Note that the sampling rate bits may not be set correctly by some test equipment causing the internal XTAL clock to become active erroneously when receiving 32 or 48KHz data even through the function should only work at 44.1KHz.

Digital filter and DAC

The serial digital audio is processed by a Yamaha YM3434 digital oversampling filter, Z206. This increases the sampling rate by a factor of four in order to simplify the subsequent analogue filtering after the DAC stage. Z206 is synchronized to the 16.9344MHz (for 44.1KHz data sampling rate) clock signal recovered by Z205.

The oversampled digital audio data is decoded into a corresponding analogue current source by Z207.

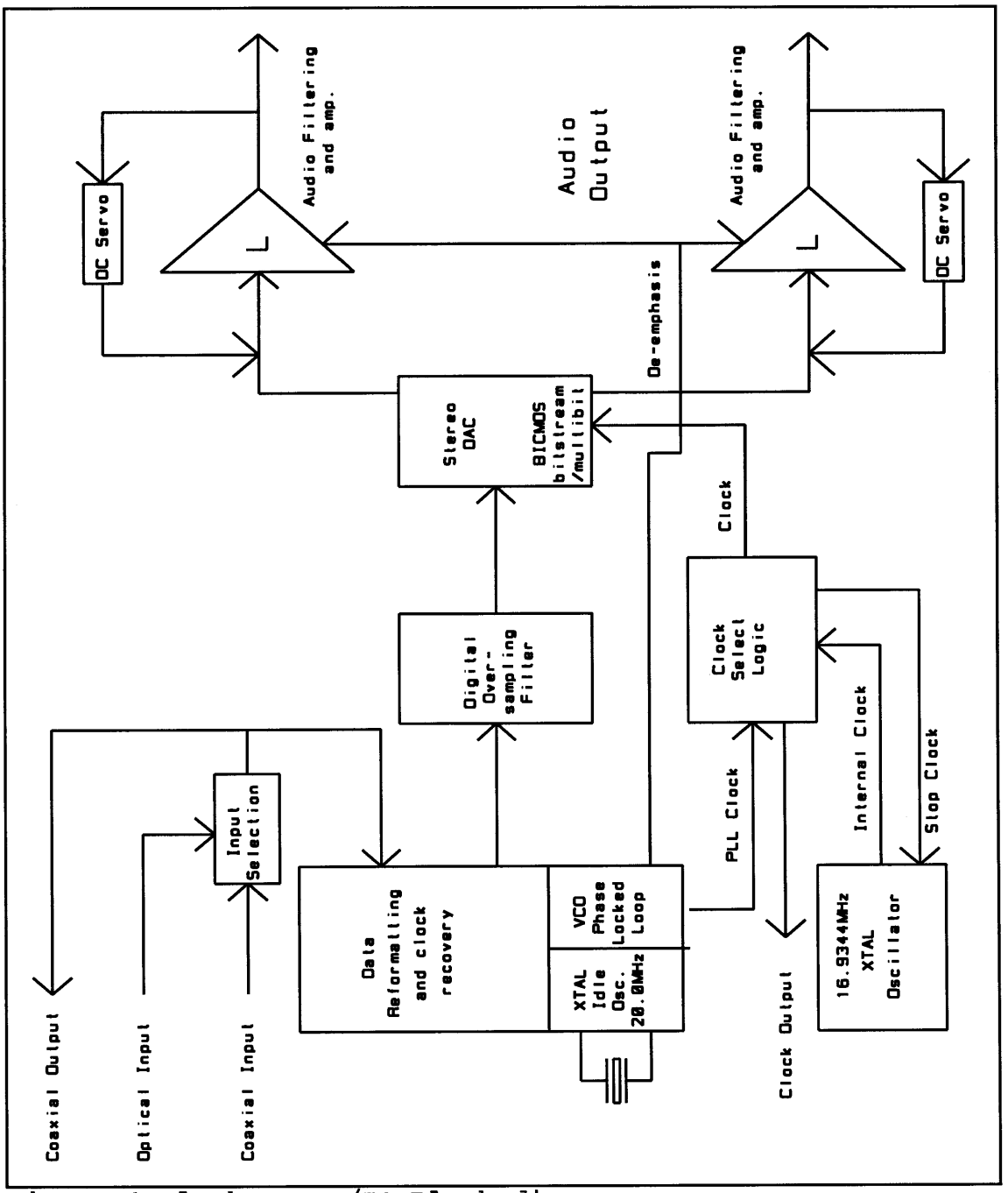


Figure 1 Black Box 5/50 Block diagram

Audio Section

Z1-A is configured to amplify the current source output from the DAC to produce a voltage level output. C5 in the feedback loop acts as the first stage of anti-alias filtering. A passive low pass filter, R6 and C8, provides another stage of anti-aliasing filter. The passive filter network C6,R7 and C7 may be switched into the signal path when Q1 is switched on. This is done when de-emphasis is required.

Z1-B buffers the output from the second stage filter/de-emphasis to drive audio line outputs directly.

D.C. Servo

To avoid the use of electrolytic capacitors in the audio signal path, Z200 is configured as a d.c. servo integrator to ensure that the audio line output is always kept at a mean d.c.

level of 0V. The d.c. error signal controls a current source, Q2, which applies current to the current node at the input of Z1-A so as to ensure no d.c. voltage offset at the line outputs.

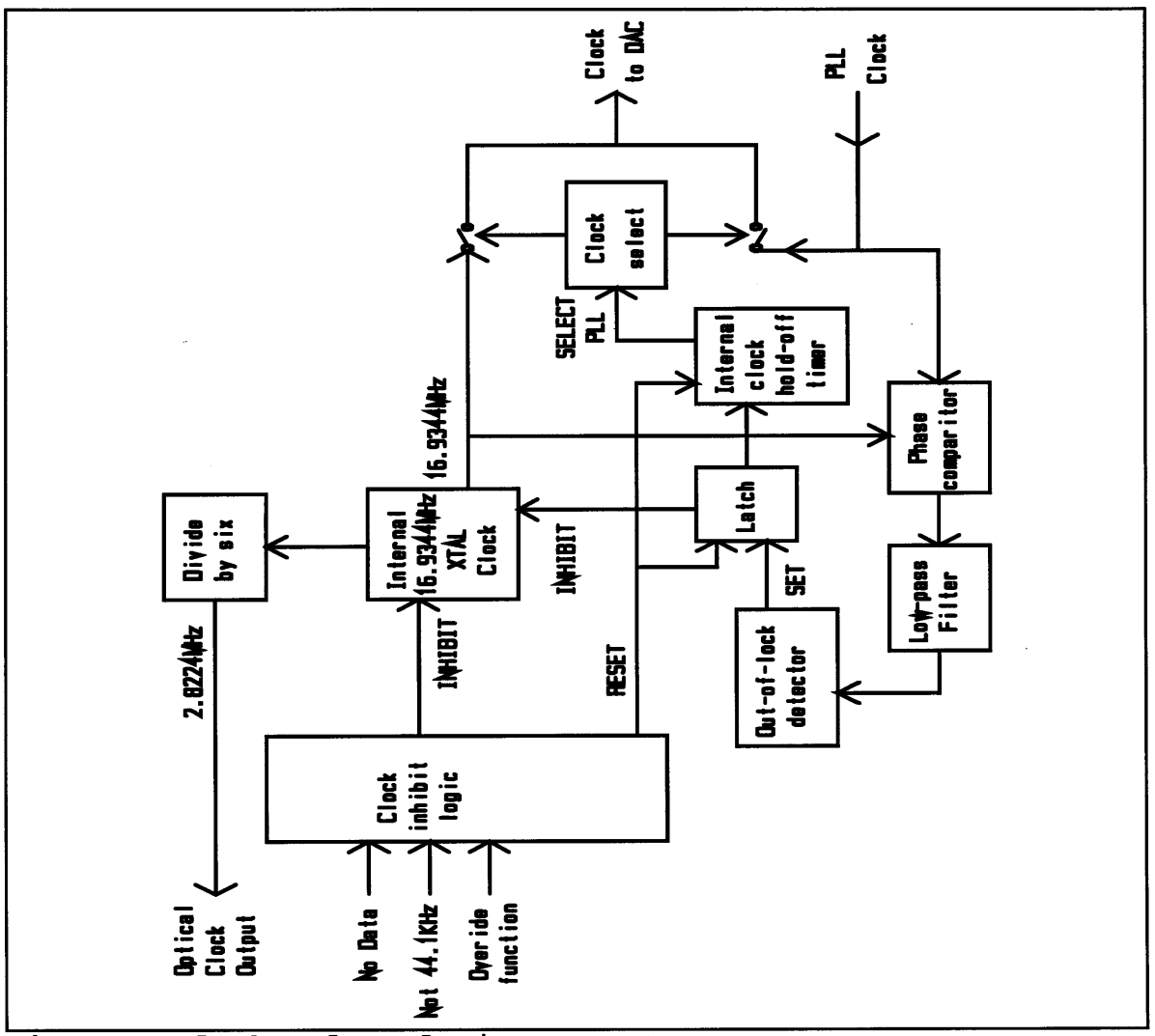


Figure 2 Clock Select logic

INT/EXT Clock Circuit

During normal operation, Z205 recovers a synchronizing clock signal from the digital audio data circuit using a phase locked loop. The recovered clock will be phase modulated by noise acquired between the original clock source in the digital data source, the connecting cable and the clock extracting circuit. This type of noise has been found to affect the sound quality performance of DACs. The solution to the problem here is to provide the DAC, Z206, with a clean clock signal directly from a crystal oscillator, Z217-A. This clock signal is divided by six by Z214-B and Z215 to a frequency low enough to be transmitted via an optical TOSLINK, Z216, to synchronize the digital data source (e.g. the D170.3) to this new clock reference.

Since not all digital data inputs have provision for an external clock source, it is necessary to determine whether the digital data will or will not synchronize to the Z217 clock. Also there is only a one crystal for use at a sampling rate of 44.1KHz. If the data is not at a sampling rate of 44.1KHz or will not synchronize, then the internal clock, Z217, must be disabled and normal operation using the PLL clock must be restored.

The sampling rate can be determined by Z205 from flags which are set in the incoming audio data. If valid data is being received at 44.1KHz, then a test is made to determine whether the data is synchronized to the internal clock signal as it is sent out via the optical link, Z216. This is done by comparing the internal clock with the PLL clock via a phase comparitor, Z204-D. When the output is filtered by R218, C225, R219 and C226, the output will be a steady d.c. value if the two clocks are at a constant phase difference. If there is any difference in clock frequency, then the phase between the two signals will cycle from 0 to 360 degrees resulting in a triangle waveform being produced from the phase detector. This is amplified by Z212-A & B to produce pulses at a frequency equal to the frequency difference between the two clocks.

C229, R225 and Z212-F, E & D hold Z214-A in a reset condition for a short time after valid 44.1KHz data is detected. After this time, any pulses produced by the phase detector, indicating different clock frequencies, cause Z214-A to latch and inhibit the internal clock. If Z214-A does not latch after a time determined by R227 and C234, then the internal clock is selected for use by the DAC via Z213.

MOTHER BOARD

Control circuitry (circuit diagram sheet 1)

The Black Box 5/50 can be set to default to either co-axial or optical inputs on power up by the setting of the switch, accessible via a hole in the rear panel.
With the switch out the co-axial input is automatically selected because the "set" input of flip flop Z301 is high and so the Q output, pin 5,is also high. This then switches in one section of the electronic switch Z304 (74HC4066) and the "digital" led is illuminated via current limit resistor R309.
If the switch is in then the "set" input initially receives a low input until C304 charges and the Q output is set low.The Schmitt invertor Z302-E (74HC14) converts the low to a high and switches in the electronic switch to turn on the "optical" led.
Once the unit is powered up the digital or optical input is selected by taking the "set" input low to select "digital" or the "reset" low to select "optical".
Note:- If the unit is switched off and on again before voltages within the Black Box have discharged, (around 5 seconds), this may give rise to apparent faulty working of this circuitry.
The output of the flip flop (pin 5) and its inverted level from the Schmitt invertor also goes to the bitstream board via a 14 way connector.

The "phase" select works in a similar way to the digital/optical select by providing a change of clock state via the Schmitt invertor Z302-B. With each push of the "phase" switch the output of the flip flop changes state and via electronic switches, Z304-B and C, turns on the appropriate bicolour led (green for normal phase).
The "phase" output also goes to the digital board via the 14 way connector.

For the output relay to open pin 6 of Z302-C must be high to turn transistor switch Q300 on. In the absence of digital data the mute VCO line, from the digital board goes high, causing pin 6 to go low and so mute the audio output.
Switching between optical and digital (co-axial) inputs also causes the relay to close to minimise switching noise. This is achieved by changing the state of pin 2 of Z302-A by taking pin 1 low via the front panel switches.

Power supplies (circuit diagram sheet 2)

The Black Box 5/50 has two mains transformers - one for the digital supplies and the other for the analogue stages.

The output of the digital transformer is rectified by diodes D207-D120 to provide a +12V unregulated supply and then regulated to +5V by the 78 series regulator Z201.
The analogue transformer output is rectified by D201-D204 to provide +/- 25V rails which are then smoothed by C201, C202, C221, C222.
The power supply earth is connected to chassis earth via R209 and C223.

The +/- 16V rails are regulated by Q201-204 and Q205-208 respectively. Zener diodes D205 and D206 with the V_{be} of Q203, Q207 provide the appropriate reference voltages.
The +5V regulated supply is used to power the TTL IC's in the control circuitry (sheet 1).
The unregulated 12V is used to power the front panel led's via suitable current limit resistors and also the mute circuit and relay.
The 12V line also goes to the digital board via the 14 way connector.
The output relay mutes the output on switch on to prevent unwanted thumps or clicks being transmitted to other equipment. The length of the switch on delay is controlled by the components around Z303 (see sheet 1).

Board Connections

SK1 Phono digital audio coaxial input, SPDIF standard

SK2 Phono digital audio coaxial output, SPDIF standard

SK3 Power and control connection to Black Box/pre-amp motherboard.

pin 1,2	-	Power, +12V unregulated DC power supply input
pin 3,4	-	Power, Digital section 0v power return
pin 5	-	Input, DIG1, selects Coaxial input when low, 8K2 pull-up to +5v.
pin 6	-	Input, DIG2, selects Optical input when low, 8K2 pull-up to +5v.
pin 7	-	n/c
pin 8	-	Input, PHASE, inverts phase of audio output when high, 8K2 pull-down to 0v.
pin 9	-	n/c
pin 10	-	Input, MUTE/OVRIDE, Overrides internal XTAL clock when high, 8K2 pull-down to 0v. Was a 'mute audio' line on Black Box 3 decoder board.
pin 11	-	Output, LOCK, Signals 'using internal XTAL clock' status to motherboard when low. Needs pull-up.

SK4 Audio connection to motherboard

pin 1,2	-	Left audio output
pin 3	-	Analogue ground
pin 4,5	-	Right audio output
pin 6	-	n/c

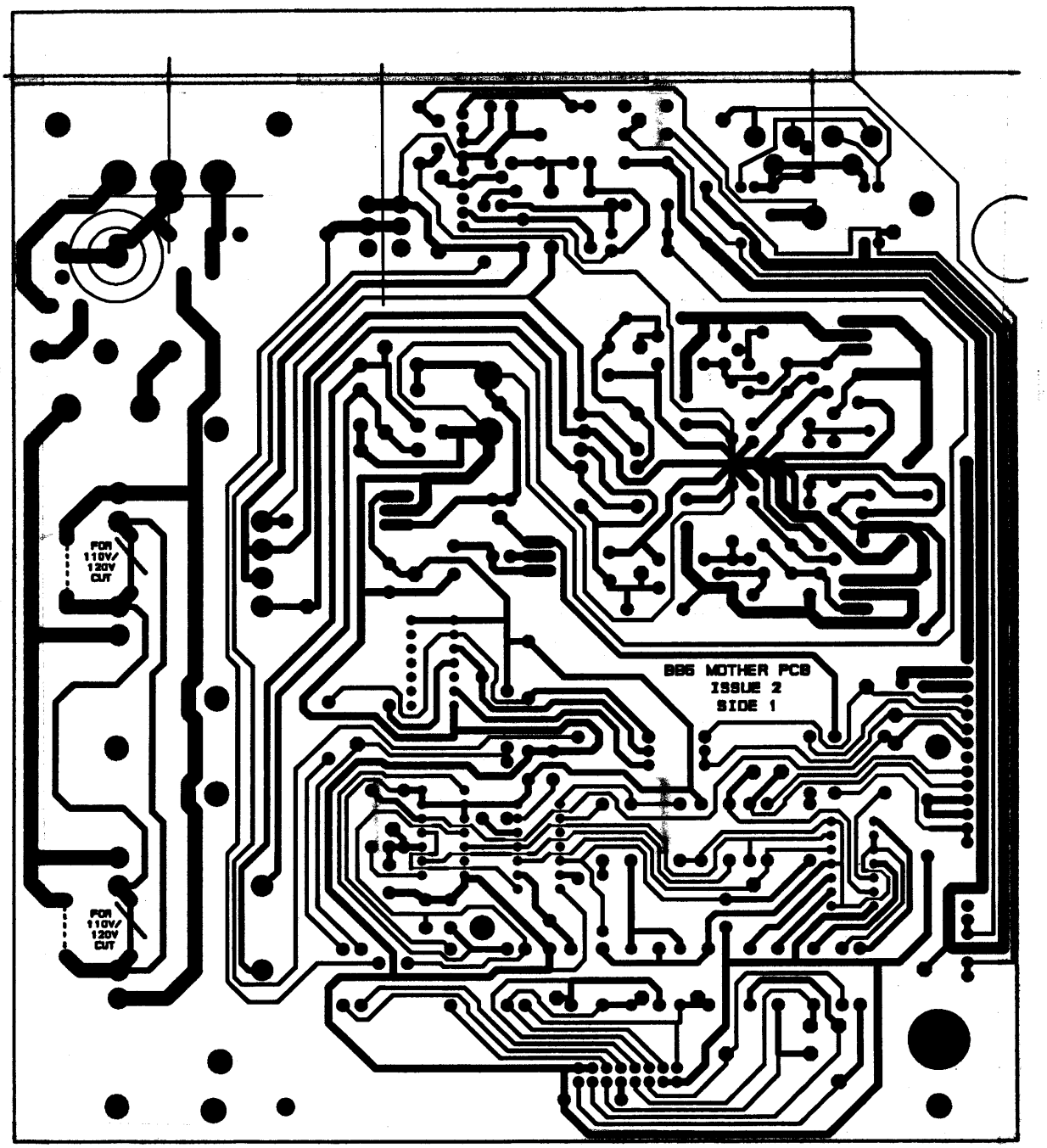
Z202 TOSLINK RX optical digital audio input

Z216 TOSLINK TX optical internal XTAL clock output

Change of Mains Voltage

WARNING - The unit must be unplugged from the mains supply when changing the wiring or the mains fuse since the fuse is at mains potential even with the unit switched off.

To convert the Black Box 5/50 to work at a different mains voltage requires cutting 2 tracks under the main pcb and adding 2 links (marked ----) (See diagram below).
Note: these links **must** be fitted to the underside of the pcb as they will be at mains voltage when the unit is plugged in. The mains fuse value remains the same (250mA anti-surge).



Disassembly for Service

Removal of input board

1. FOR BB5 ONLY: Remove 3 screws from the top edge of the rear panel and remove the top plate.
   FOR BB50 ONLY: Remove the cover by removing 4 side screws & 4 rear panel screws.

2. Undo 2 screws from rear panel holding the digital board in place.

3. Squeeze the tops of the two pcb pillars at the front edge of the input board and pull the pcb upwards of the 2 connectors and pcb pillars.

Removal of mother board

Remove the digital board as described above.

1. Remove the screw from the centre of the audio output sockets and from either side of the mains inlet socket.

2. Remove 4 screws from the mother board.

3. Release the cable to the display board.

4. Squeeze the top of the pcb pillars and pull the board upward out of the chassis.

5. If required unsolder the brown wires to the mains switch in order to remove the mother board totally from the chassis.

DIAGRAMS
Digital PCB: Input Stage
Digital PCB: INT/EXT Clock
Digital PCB: Audio Output
Mother PCB: Control Circuit
Mother PCB: Power Supplies